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In the Claims

Please cancel claims 1 through 16 and substitute claims 17 through 46 as follows:

Claims 1 through 16 (canceled).

17 (new). A program for responding to an input-output request from a host to effect a transfer to a specified location within a logical volume in a disk array storage device wherein a host operating system utilizes a first, uniquely identified base unit control block corresponding to the logical volume to effect a transfer in response to the input-output request, said program enabling the host to send overlapped input-output requests to the logical volume and comprising:

- A) a host parallel access application operable within the host including:
 - i) a first host module for defining at least one related, uniquely identified unit control block that identifies the logical volume including the establishment of a parallel access control block for each unit control block associated with the logical volume and a parallel access main control block for the logical volume through

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- which each of the base and related unit control blocks can be identified, and
- ii) a second host module for interrupting the operating system response to the input-output request including a process that assigns one of the base and related unit control blocks to the input-output request, and a process that returns control of the response to the input-output request to the operating system identifying the assigned unit control block whereby the host operating system can issue overlapped input-output requests to the given logical volume, and
- B) a plurality of facility modules operable within the disk array storage facility including:
- i) a first facility module that establishes a table for the logical volume with entry input-output requests and corresponding parameters, and
 - ii) a second facility module that tests the parameters for each new input-output request to the logical volume with respect to the parameters for input-output request entries in the table to determine which, of a plurality of control functions including enabling the

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processing of the input-output request by the
storage facility, will be performed.

18 (new). A program as recited in claim 17 wherein each input-output request specifies an address range as a parameter, said second facility module in the disk array storage device including a process that compares the address range in the new input-output request with the address range of each input-output request in the table.

19 (new). A program as recited in claim 18 wherein each input-output request includes other parameters and wherein said second facility module in the disk array storage device includes a process that compares each of the other parameters of the new input-output request with the corresponding parameters of the input-output requests in the table.

20 (new). A program as recited in claim 19 wherein a second parameter defines an input-output request that requires the entire logical volume to be dedicated to that input-output request and said second facility module includes:

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- i) a process that terminates the response to a first value of the second parameter in an existing input-output request in the table, and
- ii) a process that places the input-output request on the overlap polling queue in response to a first value of the second parameter in the new input-output request.

21 (new). A program as recited in claim 20 wherein a third parameter has a first value that defines an input-output request to be processed without interruption, said second facility module in the disk array storage facility including:

- i) a process that places the new input-output request on the overlap polling queue if the third parameter for either the new or existing input-output request has the first value, and
- ii) a process that enables the comparison of the addresses in the input-output requests if neither of the new and existing input-output requests has the first value of the third parameter.

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22 (new). A program as recited in claim 17 wherein said second host module includes:

- i) a process that monitors each input-output request from the host, and
- ii) a process that diverts control to said assignment step when said input-output request is to the logical volume.

23 (new). A program as recited in claim 22 wherein said first host module includes:

- i) a process that identifies a non-busy one of the base and related unit control blocks, and
- ii) a process that assigns the input-output request to the non-busy one of the base and related unit control blocks.

24 (new). A program as recited in claim 23 wherein said second host module includes a process that responds to each input-output request when all the base and related unit control blocks are busy by assigning the input-output request to the base and related unit control blocks in a predetermined order.

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- 5 (new). A program as recited in claim 17 wherein the disk array storage device causes an interrupt in the host upon completing a transfer and said step of diverting control establishes a parallel access mode of operation, said second host module including a process that returns control responding to the receipt of the interruption by processing the request prior to returning control to the operating system.
- 26 (new). A program as recited in claim 17 wherein the establishment of a parallel access control block by said first host module includes substituting the address of that related unit control block for the base unit control block contained in the input-output request and wherein said assignment process in said second host module substitutes the address for the base unit control block in the input-output request.
- 27 (new). A program as recited in claim 17 wherein each input-output request includes at least a first command with starting and ending addresses and wherein the host additionally optimizes input-output requests with:

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- i) a process that intercepts the input-output request before a command transfers to the data storage facility,
- ii) a process that scans each command in the input-output request for determining each starting and ending address,
- iii) a process that converts the scanned addresses into starting and ending addresses for an address extent that is coextensive with the collective command starting and ending addresses of the input-output request, and
- iv) a process that transfers the extent starting and ending addresses with the first command to the data storage facility.

28 (new). A program as recited in claim 27 wherein said converting process that selects the lowest starting address and the highest ending address of any command in the input-output request.

29 (new). A program as recited in claim 28 wherein said converting process initializes a starting address register and an ending address register and replaces the contents

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of the starting and ending address registers when one of the starting and ending addresses of a command are less than and greater than the value in the corresponding one of the starting and ending address registers.

30 (new). A program as recited in claim 29 additionally comprising a process that compares the starting and ending address in the first command with the corresponding value in the starting and ending address registers.

31 (new). A program as recited in claim 27 additionally comprising a process that replaces a write intent entry in the first command when the input-output request is devoid of any write commands.

32 (new). In a data processing system in which a host responds to an input-output request by effecting a transfer to a specified location within a logical volume in a disk array storage device wherein a host operating system utilizes a first, uniquely identified, base unit control block corresponding to the logical volume to effect a transfer in response to the input-output request, apparatus for

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enabling the host to send overlapped input-output requests
to the logical volume and comprising:

A) within the host

- i) at least one related, uniquely identified unit control block that identifies the logical volume and a parallel access control block for each unit control block associated with the logical volume and a parallel access main control block for the logical volume through which each of the base and related unit control blocks can be identified,
- ii) interrupting means for interrupting the operating system response to the input-output request by assigning one of said base and related unit control blocks to the input-output request, and
- iii) return means for returning control of the response to the input-output request to the operating system identifying the assigned unit control block whereby the host operating system can issue overlapped input-output requests to the given logical volume, and

B) within the disk array storage facility

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- i) a table for the logical volume with entry input-output requests and corresponding parameters, and
- ii) parameter testing means for testing the parameters for each new input-output request to the logical volume with respect to the parameters for input-output request entries in said table to determine which, of a plurality of control functions including enabling the processing of the input-output request by the storage facility, will be performed.

33 (new). A data processing system as recited in claim 32 wherein each input-output request specifies an address range as a parameter, said parameter testing means in the disk array storage device including means for comparing the address range in the new input-output request with the address range of each input-output request in the table.

34 (new). A data processing system as recited in claim 33 wherein each input-output request includes other parameters and wherein said parameter testing means in the disk array storage device includes means for comparing

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each of the other parameters of the new input-output request with the corresponding parameters of the input-output requests in the table.

35 (new). A data processing system as recited in claim 34 wherein a second parameter defines an input-output request that requires the entire logical volume to be dedicated to that input-output request, said parameter testing means of the second parameter including:

- i) means for terminating the response to a first value of the second parameter in an existing input-output request in the table, and
- ii) means for placing the input-output request on the overlap polling queue in response to a first value of the second parameter in the new input-output request.

36 (new). A data processing system as recited in claim 35 wherein a third parameter has a first value that defines an input-output request to be processed without interruption, said parameter testing means including:

- i) means for placing the new input-output request on the overlap polling queue if the third

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parameter for either the new or existing input-output request has the first value, and

- ii) means for enabling the comparison of the addresses in the input-output requests if neither of the new and existing input-output requests has the first value of the third parameter.

37 (new). A data processing system as recited in claim 32 wherein said interrupting means in the host includes:

- i) means for monitoring each input-output request from the host, and
- ii) means for diverting control to said assignment means when said input-output request is to the logical volume.

38 (new). A data processing system as recited in claim 37 wherein said interrupting means the host includes:

- i) means for identifying a non-busy one of the base and related unit control blocks, and
- ii) means for assigning the input-output request to the non-busy one of the base and related unit control blocks.

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- 39 (new). A data processing system as recited in claim 38
wherein said interrupting means includes means for
responding to each input-output request when all the base
and related unit control blocks are busy by assigning the
input-output request to the base and related unit control
blocks in a predetermined order.
- 40 (new). A data processing system as recited in claim 32
wherein the disk array storage device causes an interrupt
in the host upon completing a transfer and said
interrupting means includes means for diverting control to
establish a parallel access mode of operation and said
return means includes means for returning control
responding to the receipt of the interruption by
processing the request prior to returning control to the
operating system.
- 41 (new). A data processing system as recited in claim 32
wherein said a unit control block is associated with a
related unit control block and said interrupting means
includes means for substituting the address of that
related unit control block for the base unit control block

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contained in the input-output request and means for substituting the address for the base unit control block in the input-output request.

42 (new). A data processing system as recited in claim 32 wherein each input-output request includes at least a first command with starting and ending addresses and wherein the host additionally optimizes input-output requests and comprises:

- i) intercepting means for intercepting the input-output request before a command transfers to the data storage facility,
- ii) scanning means for scanning each command in the input-output request for determining each starting and ending address,
- iii) converting means for converting the scanned addresses from said scanning means into starting and ending addresses for an address extent that is coextensive with the collective command starting and ending addresses of the input-output request, and

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iv) transfer means for transferring the extent
starting and ending addresses with the first
command to the data storage facility.

43 (new). A data processing system as recited in claim 42
wherein said converting means includes means for selecting
the lowest starting address and the highest ending address
of any command in the input-output request.

44 (new). A data processing system as recited in claim 43
wherein said converting means includes:

- i) initializing means for initializing a starting
address register and an ending address register,
and
- ii) replacing means for replacing the contents of
the starting and ending address registers when
one of the starting and ending addresses of a
command are less than and greater than the value
in the corresponding one of the starting and
ending address registers.

45 (new). A data processing system as recited in claim 44
additionally comprising means for comparing the starting

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and ending address in the first command with the
corresponding value in the starting and ending address
registers.

46 (new). A data processing system as recited in claim 42
additionally comprising means for replacing a write intent
entry in the first command when the input-output request
is devoid of any write commands.